Notice of Allowability	Application No.	Applicant(s)	
	10/604,472	HUANG, SHIH-HUANG	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/23/03*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ The drawings filed on *23 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4/27/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-15 are allowed.

2. The following is an examiner's statement of reasons for allowance:

U.S. Patent No. 5,315,555 to Choi is the reference closest to the claimed invention. Choi discloses a sense amplifier for use in a semiconductor memory device, the semiconductor memory device having first and second memory blocks including a plurality of memory cells, a pair of sensing lines commonly connected to the first and second memory array blocks, through a pair of first isolation transistors and a pair of second isolation transistors isolating the first and second memory array blocks from the sensing lines when a given memory cell is selected, and a pair of common input/output lines for transferring input/output data to an exterior of a semiconductor memory chip, and data input/output transistors connected between the sensing lines and the common input/output lines, comprising a precharge means connected to the sensing lines positioned between the first and second isolation transistors, for precharging voltage of the sensing lines to a power voltage level by a given control signal, and a sensing means connected to the sensing lines, for amplifying a potential difference between the sensing lines, wherein the precharging means is operated only when the control signal is active state, and the sensing means is operated only when the control signal is non-active state. However, Choi does not teach a sensing circuit for sensing the logic data stored in a memory cell, the memory cell being electrically connected to a bit line, the sensing circuit comprising: a first pre-charging module, electrically connected to the bit line, for pre-charging the bit line; a selecting module, electrically

connected to the bit line and a first data line, for transmitting signals of the bit line to the first data line according to a first controlling signal and isolating the capacitance of the bit line and the first data line; a second pre-charging module, electrically connected to the first data line, for pre-charging the first data line; a first voltage keeping module, electrically connected to the first data line, for maintaining the signal on the first data line at a high voltage level when a logic value "1" is stored in the memory cell; an isolating module, electrically connected between the first data line and a second data line, for transmitting signals from the first data line to the second data line according to a second controlling signal and isolating the capacitance of the first data line and the second data line; and a third pre-charging module, electrically connected to the second data line, for pre-charging the second data line, and including all of the other limitations in the independent claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimoto et al. disclosea Vss precharge scheme, a dummy cell including a bit line contact, a storage node contact and a third contact connected to a Vccs power supply line being arranged in complementary bit lines respectively.

Vogelsang et al. disclose an interleaved sense amplifier with a single sided precharge device which providing simplification of the conventional sense amplifier circuitry, as well as a reduction in the area occupied by the sense amplifier circuitry, thereby resulting in chip size reduction.

Tsukude et al. disclose each of divided bit line pairs being selectively connected to a sub-input/output line pair through transfer gates.

Chi et al. disclose a pre-charge and isolation circuit for a folded bit line DRAM array to reduce noise coupling between adjacent bit lines of a DRAM array by connecting only one bit line within one sub-array to be connected to a sense amplifier, while the complementary bit line used for the reference voltage of the sense amplifier is selected from an adjacent sub-array.

Nakano discloses a semiconductor memory has a bit line connected to a plurality of memory cells and a single end type sense amplifier connected to the bit line.

Koike et al. disclose (A) at least one memory cell array, the memory cell array including (a) a plurality of memory cells arranged in row and column directions, each of the memory cells having a capacitive element and a transistor, the capacitive element having a ferroelectric film interposed between electrodes facing to each other, storing and retaining binary data in accordance with polarization of the ferroelectric film, one of a source and a drain of the transistor being electrically connected to one of the electrodes of the capacitive element, and (b) a plate line being electrically connected to the other of the electrodes of the capacitive element; and (B) an arrangement for arranging a voltage of the plate line to be fixed and activating the transistor so as to arrange a voltage at a junction of the transistor and the
capacitive element to be the same as the voltage of the plate line.

Takashima et al. disclose a dynamic semiconductor memory device according to the present invention comprising at least first and second memory cell arrays having a plurality of memory cells selectively arranged at respective intersections of a plurality of word lines and a plurality of bit lines, a first sense amplifier section connected at an end of the first cell array to a plurality of bit line pairs formed by part of the plurality of bit lines of the first cell array, the plurality of bit line pairs having a folded bit line configuration, a second sense amplifier section connected to sets of bit line pairs, each formed by one of the remaining bit lines of the first cell array and one of part of the plurality of bit lines of the second cell array, the plurality of bit line pairs having an open bit line configuration, and a correction circuit for correcting the level of ease for reading data "0" and that of reading data "1".

Kanzaki discloses a semiconductor memory device pre-charges the electric potential of a selected bit line up to a predetermined electric potential, and judges the electric potential of the selected bit line on the basis of the predetermined electric potential as a threshold value after the pre-charge.

Kaibara et al. disclose a semiconductor integrated circuit apparatus having a basic cell region formed by arranging a plurality of basic cells each including a MOS transistor in longitudinal and transversal directions.

Okitaka et al. disclose semiconductor memory device having bit lines and word lines different in data reading and data writing.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

11/02/04